Characterizing and Optimizing High Q Inductors for RFIC Design in Silicon Processes

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Abstract - **A novel metric for assessing inductor performance of advanced silicon RF process technology is proposed. The metric makes use of measured data and a verified physical model to generate a design space involving quality factor, inductance and area. Examples for technologies with top metal thickness ranging from 3μm to 6μm and dielectric thickness ranging from 4.5μm to 8.5μm are presented. Conclusions are drawn regarding the usefulness of thicker dielectrics and metal layers for RF applications in the 900MHz to 10GHz range.**

I. INTRODUCTION

Inductor characterization and performance enhancements have received a great deal of attention in recent literature. Unfortunately, most of this effort has concentrated on the optimization of the quality factor with little attention paid to what circuit designers actually consider important. As an example, these best reported Q's are often quoted at frequencies few, if any, designers care about. This focus on a single metric also masks other important application specific features of inductors. For example, in the design of handset power amplifiers, the Q factor is secondary compared to inductance per unit area except for output matching. As a result, focusing on optimizing Q is not relevant for this application. Another example is for LNA design where designers require the highest Q and lowest noise at a given resonance frequency[1]. Finally, for given applications, maximizing the Q for a given inductance value is always more important than the raw Q of some arbitrary inductance value.

A better metric to characterize inductor performance within a process is a set of inductor performance curves over specific design spaces. Such set of curves can (1) show inductor performance capabilities for a given process based on application; (2) provide an analysis of the impact of process variants; and (3) show die area impact for on-chip inductors. The conclusion of such analysis provides feedback to both an RFIC designer in selecting a process for design and to the process development engineer supporting the process.

II. RELATIONSHIP OF Q TO PROCESS DESIGN

To understand the impact of the process on the Q of an inductor, the literature can provide some basic insight using simplified equations and the simple model shown in Fig 1. If the substrate is ignored (i.e. $Tox \rightarrow \infty$), the performance of an inductor is fundamentally given by:

$$Q = \frac{\omega L}{R} \tag{1}$$

The three parameters affecting the Q are the frequency, inductance, and resistance; however, an RFIC design will typically require a specific frequency and inductance for the application. Thus, the quality factor becomes more directly controlled by the resistance and application. A high Q inductor for a non-existent application or one that sacrifices other critical parameters such as area or process complexity provides little value.

To examine the performance of an inductor including substrate, one can look at the two port Y parameters. In a single ended tank circuit, the Q is given by:

$$Q = \frac{-\text{imag}(y_{11})}{\text{real}(y_{11})} \tag{2}$$

The oxide capacitance and substrate resistance will cause the Q curve to roll over at some peak frequency as the capacitance adds a low impedance path through a lossy substrate. Therefore, the straight line equation with frequency (from when we initially ignore skin effect), starts to deviate at the point where the capacitance(s) become significant. The Q starts to deviate from (1) and rolls over until it reaches zero (Fig 2) where the impedance of the inductance is equal to the impedance of the capacitance (i.e. self-resonance frequency or SRF). Thus by decreasing the capacitance, the point of roll-over increases and the usefulness of the inductor is extended to higher frequencies. Alternatively, SRF and capacitance roll-over can provide the ability to build a specific inductor with a specific Q for a given application. Thus, for a given application (selected ω and L), the point of roll-over is critical.

Given this relationships between resistance and capacitance, the impact on process selection for an RFIC designer or process development for a device engineer can be

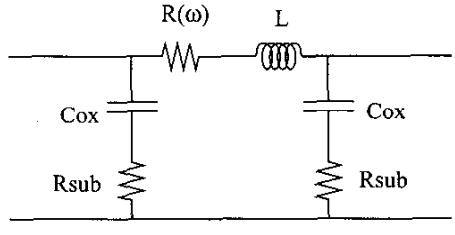

Fig 1. Simple circuit model for an inductor.

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addressed. A circuit application will set the value of L and frequency, thus the best inductor is determined by the metal resistance and the roll-over caused by the capacitance. To obtain the highest possible Q requires that the slope given by (1) and designated in Fig 2 as Rdc needs to be as large as possible. Since the application is given, that slope is purely dictated by the resistance. Two approaches reduce resistance: thicker metal and wider metal lines.

Process development can be used to increase the thickness of the top metal. The improvement one gets can be modeled based on [2] which incorporates the skin effect into the resistance equation. For a frequency of 5GHz (wireless LAN application) with AlCu for the top metal, Fig 3a shows that the improvement one obtains saturates for a metal thickness of around 6μm.

Wider metal lines can improve inductor performance without process changes, but the advantage of using wider metal lines has it's limitations due to skin effect and proximity effect. As metal lines get wider, the inductance per unit length is reduced and proximity effects will not allow the resistance of the lines to scale linearly. Fig 3b shows the improvement of Q given by (1) versus metal width using a model based on [2] and [3]. In addition, the area and capacitance increase with metal area thereby reducing the frequency at which peak Q rolls over and thus, the usefulness of the inductor.

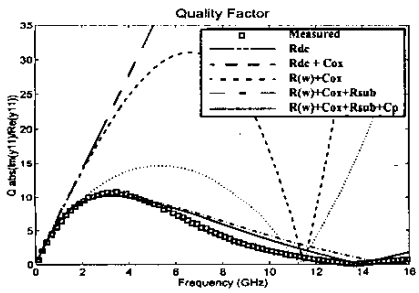
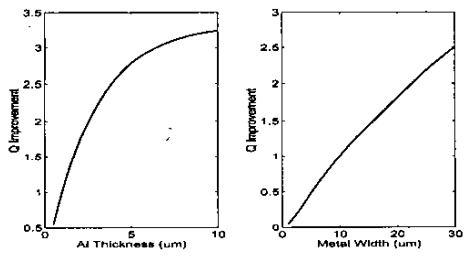


Fig 2. Typical Q curve of inductor showing impact of various physical components in a Si process.



(a) (b)

Fig 3. Relative impact of (a) metal thickness and (b) metal width on inductor Q at 5GHz.

III. MEASURED AND MODEL DATA

Having done the initial analysis based on simplified equations, a more complex study is done with measured inductor data and a validated inductor model to explore process regions. A physics based model that includes skin effect and substrate loss is used to evaluate inductor performance in different process variants (Fig 4)[4]. The model has a resistor ladder to represent the skin effect of the metal. The model has a substrate network to represent the impact of the substrate with the assumption that a perfect RF return path exists 100μm from the inductor. The coupling capacitance represents the cross-over and inter-winding capacitance. Most importantly, the via resistance and underpass resistance (Rpass) is included in the model since both these effects are critical factors in the physical realization of the inductor.

Besides the model, a test chip with approximately 1000 inductors with sizes ranging from 80μm x 80μm to 450μm x 450μm has been created. The inductors on the test chip represent the structures that an RFIC designer would reasonably select for applications such as VCO design, LNA design, mixer design, transceiver design, filter design, etc. at frequencies from 500MHz to 10GHz. The test chip is designed to work within a short-loop back-end flow that represents the regular process flow to allow fast characterization and experimentation. This short-loop process has been validated against a full flow BiCMOS process.

The physics based model has been validated using data from multiple process variants with top metal thickness ranging from 3μm to 6μm and dielectric thickness ranging from 4.5μm to 11μm [4]. Thus, both the model and measured data become valuable tools for evaluating the impact of process design for an inductor in a specific RFIC application.

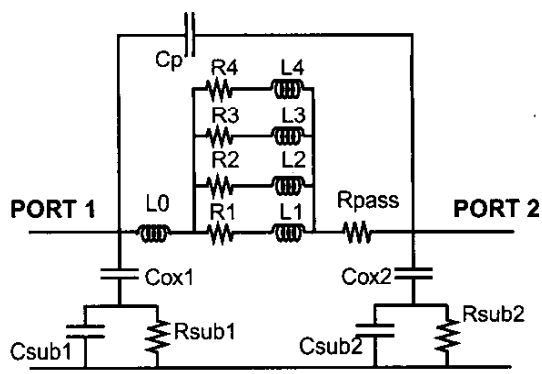


Fig 4. Physics based inductor model.

Fig 5 shows sample of the fit of the model compared to measured data from two different process variants.

IV. INDUCTOR DESIGN SPACES FOR RFIC's

Rather than quoting a single peak Q value, a much better metric to characterize the performance of inductors in a process is to plot the attainable Q's for specific RF applications. Fig 6 contains points for the modeled peak Q of individual inductors from the test chip. The lines represent the center of the inductor design space for different RFIC applications. This version of the process contains 6μm of AlCu on 8.5μm of oxide dielectric over a typical SiGe substrate. The applications are divided into 900MHz (analog cellular), 1.8GHz (digital cellular), 2.45GHz (networking, digital cellular, bluetooth), 5GHz (wireless LAN), and 10GHz (networking). To validate against measurements, a similar plot from measured data from the inductor test chip is shown in Fig 7.

The curves are important for evaluating and comparing process capability. For example, Fig 8 contains the inductor curves for a process with 3μm of AlCu on 6.9μm of oxide dielectric. The Q advantage gained from the thick AlCu (Fig 8) by process improvement is clearly obvious from comparing the charts. In addition, the family of design spaces provides information on the available inductors in each process. For example, such a family shows the difficulty in building a high-Q 3nH inductor at 5GHz in either process, but a 3nH inductor at 2GHz shows significant difference. By comparing specific applications, it becomes possible to better select a process option for RFIC design or direct development of a process for high-Q RFIC applications.

V. PROCESS SELECTION

Individual applications should be considered when determining which process provides the biggest advantage. Consider high performance VCO applications at 1GHz, 2GHz, and 5GHz. Table 1 shows a subset of the capabilities of different processes using the validated inductor model with 3 different dielectric thickness and 3 different metal thicknesses. Note that the impact of the underlying underpass metal is included and is 0.6μm of AlCu. In the first column, the maximum available Q from the process is presented; in the second column the area required to obtain that Q is provided; and in the third column the area required for a constant Q inductor is found. Note that N/A implies the process variant is not capable of having such an inductor. By using a Q of constant value, the footprint of the inductor shrinks with each new advancement in process design. If a circuit requires many inductors, the area savings could be

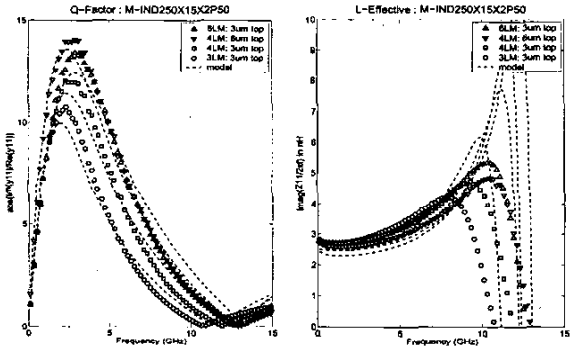


Fig 5. Measurements versus a physic based inductor model for various back-end metalization schemes.

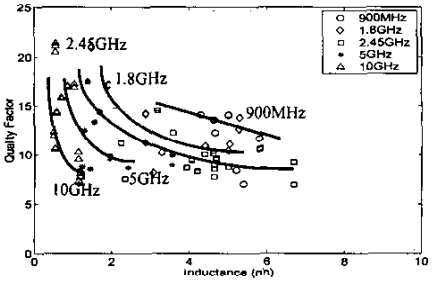


Fig 7. Measured Q's in process with 6μm of Al and 8.5μm of oxide.

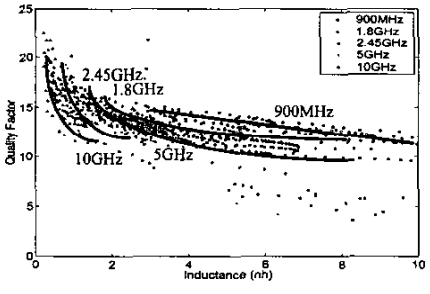


Fig 6. Modeled Q's in thick metal process of 6μm of Al and 8.5μm of oxide.

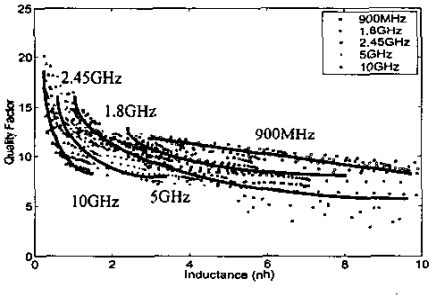


Fig 8. Modeled Q's in process with 3μm of Al and 6μm of oxide.

Table I: OPTIMIZED INDUCTORS IN VARIOUS BACKEND METAL PROCESS VARIANTS

Process		900MHz VCO (L=5nH)			1.9GHz VCO (L=3nH)			5GHz VCO (L=1nH)		
Tmetal	Toxide	Max(Q)	X(max)	X(Q=10)	Max(Q)	X(max)	X(Q=12)	Max(Q)	X(max)	X(Q=14)
3	4.69	9.2	320	N/A	9.6	210	N/A	12.2	150	N/A
3	6.69	10.8	350	290	11.2	240	N/A	13.7	170	N/A
3	8.69	12.0	380	270	12.4	250	230	15.0	180	150
3	10.69	12.8	410	260	13.4	300	220	16.9	200	140
6	4.69	11.3	290	200	11.6	190	N/A	13.9	150	NaN
6	6.69	13.0	350	190	13.0	200	160	15.5	160	130
6	8.69	14.5	360	180	14.3	240	150	16.9	180	110
6	10.69	15.5	370	180	15.5	250	150	18.2	190	110
9	4.69	12.8	250	140	13.1	170	110	15.1	140	90
9	6.69	13.9	260	140	14.4	170	110	16.8	170	80
9	8.69	14.9	280	140	15.1	170	100	18.3	170	80
9	10.69	15.8	300	130	15.6	180	100	19.2	170	90f

more important aspect for the RFIC design than the maximum attainable Q. The table clearly shows the point of diminishing returns in area with the limited variants in metal thickness and dielectric thickness. A much better representation of the data is shown in Fig 9. For example, the graph shows that for an analog cellular design requiring an inductor with a Q of 10 it is possible to shrink the area of the inductor by increasing the dielectric thickness for a 3µm top metal, whereas dielectric thickness has very little impact for a 9µm top metal. It also shows that increasing the metal thickness not only improves Q but can also reduce area significantly.

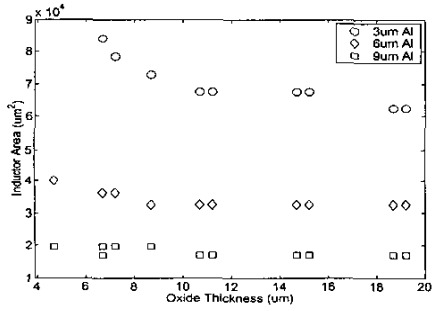


Fig 9. Inductor (Q=10) area for a 900MHz application in different process variants

CONCLUSIONS

A new metric has been developed and demonstrated for evaluating inductors in RF silicon processes. The metric relates inductor quality factor, area, and inductance for the specific application for which it is to be used. Specific examples were shown for RFIC design spaces spanning 900MHz to 10GHz with process variants for metal thickness from 3um to 6um AlCu on top of 4.5um to 8.5um of oxide. The characterization described provides a method to better understand inductor design as a function of process and allows for optimization when weighing the trade-offs of inductor performance and RFIC application.

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